REMARKS

The specification has been amended in order to resolve obvious errors. No new matter was added.

The Applicants would like to thank the Examiner for the telephone interview conducted on February 1, 2007. During the interview the Applicants stated that the write buffer in the Zumkehr patent, Patent No. 6,901,494, does not disclose a bypass data path having a write bypass circuit coupled to a direct data pass operable to temporarily store the write data to allow read data to be transferred through the direct data path. The Examiner did not agree. The Examiner suggested that the Applicants draft an argument for his Supervisor to review. The Applicants would like to thank the Examiner and his Supervisor for the opportunity to have the argument reviewed by the Examiner's Supervisor.

After the interview, Applicants' attorney spent a great deal of time studying the Zumkehr patent and now has a better understanding of the Examiner's position. Applicants admit that there are some similarities between subject matter disclosed in the present application and the Zumkehr patent for situations in which the write data is passed from the controller 210 to the translator hub 220 *before* a read command is applied to the hub 220. For example in Zumkehr, write data is passed from the controller 210 to the translator hub 220 before a read command is passed from the controller 210 to the translator hub 220 and from the translator hub 220 to the appropriate memory device 161. The read data is then passed from the memory device 161 to the translator hub 220. A write command corresponding to the previous write data is then sent from the controller 210 to the translator hub 220. During the time the read data is being sent from the translator hub 220 to the controller 210, the write data also is sent from the translator hub 220 to the appropriate memory device 161. Therefore, data is being transferred on the bus at the same time. *Zumkehr Specification*, Figure 5B and column 6, lines 53-67 - column 7, lines 1-49.

On the other hand, there are differences that are significant for situations where, as in applicants' system, the write command and corresponding write data are output from a controller *after* the read command are output from the controller. In the Zumkehr system, when a read command is issued to the memory system before a write command and corresponding write data are issued to the memory system, the controller 210 defers the transfer of the write data from the controller 210 to the translator hub 220 until the read latency is met. *Zumkehr*

specification, column 7, lines 15-20 and Figure 5B. The disclosed system, however, does not require that the read latency be met before transferring the write command and corresponding write data from the controller to the memory system. Rather, the write command and corresponding write data may be provided to the memory system after the read command is issued to the memory system. This means that read data will be going in one direction to the controller and write data will be going in the opposite direction to a memory device at the same time. In order to prevent a collision on the data bus, the write data is decoupled from the bidirectional data bus by the bypass register. Once the read data has passed the bypass register, the write data is recoupled to the bidirectional data bus. Because the Zumkehr patent requires the write data to be already stored in the hub before a read command is issued, it does not meet all of the requirements for the method claims in the present application.

The Applicants propose canceling the apparatus claims, 1-4, 11-15, and 21-25 in the present application. The Applicants further propose filing a continuation application to prosecute amended apparatus claims separately from the method claims of the current application. In addition, the Applicants propose amending independent method claim 32 in the present application so that it has limitations similar to those already included in independent method claims 36 and 40, that the read command is issued to the memory system before the write data is provided to the memory system.

Upon the Examiner's acceptance of the proposed changes, all of the claims remaining in the application are clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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